

Abstract of the Disclosure:

In a method for operating a PLL frequency synthesis circuit, the circuit is in an active state and synthesizes a first output frequency during a first data transmission period. The 5 circuit is likewise active and synthesizes a second, different output frequency during a later, second data transmission period. The PLL frequency synthesis circuit is first reprogrammed to an intermediate frequency, and is controlled from there to the second output frequency, in an intermediate 10 time period.

REL/nt